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Applicant:	Grutzediek et al.	Confirmation No.:	4906
Serial No.:	09/806,224	Examiner:	Suk San Foong
Filed:	06/11/2001	Group Art Unit:	2823
Title:	Method for Producing Transistors		

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 5, 2003.

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REQUEST FOR RECONSIDERATION

Dear Sir:

This Request is being submitted in Response to the Final Office Action Dated March 7, 2003, and is accompanied by a Petition for a Two-Month Extension of Time and a Request for Continued Examination. The extended response period expires on August 7, 2003. Accordingly, this Request is timely filed.

In the Final Office, claim 1 was rejected under 35 U.S.C. 102(b) as allegedly anticipated by Sakurai et al. ('022) and claims 2-30 were rejected under 35 U.S.C. 103(a) as allegedly obvious over Sakurai et al., further in view of official notice or Nemoto ('551), as previously

applied. These rejections are respectfully, but most strenuously traversed, for the reasons presented below.

An important aspect of the present invention, as defined by independent claim 1, is the production of a trough in a semiconductor substrate with an ion implantation energy that maintains the original type of doping of a doped inner area on a surface of the substrate. For example, an N-doped trough is placed in a P-doped semiconductor substrate by means of ion implantation through a mask using an energy that assures a P-doped inner area remains on a surface of the P-doped semiconductor substrate (conversely, a P-doped trough can be produced in an N-doped semiconductor substrate by means of ion implantation through a mask using an energy that assures that an N-doped inner area remains on the surface of the N-doped semiconductor substrate).

Applicant's Amendment dated December 12, 2002 and specifically incorporated by reference herein, explains how Sakurai's improved method, as illustrated in Figures 7-13 of that patent, explicitly requires an additional compensation step to revert an inner surface area to the doping of the original substrate. According to the present invention, this additional method step is not necessary since the doping in the inner surface area does not change when the trough is formed.

In response to this argument, the Examiner, in the Final Office Action, directs Applicant to Figs. 2-6 of the Sakurai et al. patent wherein allegedly "trough 24 is formed without changing the conductivity type of the inner area".

Applicant respectfully submits that the Examiner's latter contention is mistaken.

The introductory part of Sakurai (Column 2, line 20-Column 4, line 1) makes reference to a prior art method for producing semiconductor components. It should be noted that only the broad method steps are described in this introductory part of the Sakurai patent, making reference to Figures 2-6 of the patent.

In the example presented in the introductory part of the Sakurai patent, a N^+ -type buried layer is formed by phosphorous ions implantation in a P-type silicon semiconductor substrate 21. The general description of this earlier method in the Sakurai et al. reference does not specify the implantation energy used to create the N^+ -type buried layer 24 in the P-type semiconductor substrate 21, but does describe the region 26 surrounded by the N^+ -type buried layer 24 as P-type. Thus, the Examiner is inferring from this general description of the earlier method that an

implantation energy is employed that leaves a trough enclosed surface area with the same doping as the original substrate.

At page 2, lines 20-25, Sakurai states that the described earlier method was proposed in Japanese Patent Application No. 50-364 (application date: December 23, 1974). Accordingly, Applicant has obtained and encloses herewith a copy of this Japanese patent application and an English translation thereof.

The accompanying Japanese Patent Laid-Open No. S51-73887/76 (Inayoshi) discloses a method for producing semiconductor components, wherein an implantation energy of 1 MeV is used. Figure 3 of this reference suggests that the inner area 4 above the trough 3 retains the same donor type as the original substrate. However, using an implantation energy of 1 MeV, the donation in the upper inner area 4 actually changes. This changing of donation is referred to as "turn over of conductivity type" in this reference.

More particularly, the Examiner's attention is directed to Figure 4 of this reference and to the following paragraph 5 from the translated Japanese reference:

> For improving the performance in particular, namely for preventing turnover of conductivity type in board 1, boron ion is injected into board 1 with low concentration, and P^+ -type layer 5 is formed.

As indicated in the above quoted paragraph, an additional compensation step is necessary due to the changing in the donation in the upper inner surface area 5. This additional compensation step is required and, therefore, implicit in the description of this earlier method in the Sakurai reference. Note that Sakurai's improved method employs the identical additional compensation step.

In accordance with the present invention, the above-described additional compensation step is not necessary since the doping in the inner surface area does not change when the trough is produced by ion implantation. This feature clearly distinguishes the invention of claim 1 from the improved method of the Sakurai et al. reference as well as the earlier described method of Inayoshi, referred to in the introductory portion of the Sakurai et al. reference.

Claims 2-30 are allowable for the same reasons as independent claim 1 from which they all depend, as well as for their additional limitations. Certain of these additional distinguishing features of the dependent claims will now be described with regard to preferred embodiments of

the invention, i.e. the I^2L element (claim 10) as shown in Figures 5a to 5e, the pnp transistor (claim 5) as shown in Figures 3a to 3e and the field effect transistor (claim 13) as shown in Figures 6a to 6f.

Sakurai as well as Inayoshi are devoid of any teaching or suggestion to use the semiconductor structure according to the invention to produce the above-mentioned semiconductor elements.

Inayoshi does not disclose or even suggest an I^2L element, a pnp transistor and a field effect transistor rather than a npn transistor only (Fig. 5). As discussed above, Inayoshi does not teach to use an implantation energy that will assure that a p-doped inner area remains on the surface of the p-doped substrate. Even if Inayoshi would teach to produce the semiconductor structure according to the invention, Inayoshi does not teach or even suggest to produce an n-doped area joining the fringe area of the n-doped trough with the p-doped inner area and in the p-doped inner area at least one n-doped area for the creation of a structure forming an I^2L element.

Sakurai discloses an I^2L element (Figure 14). The method for producing the I^2L element, however, is different from the method according to the invention. For obtaining the buried layer 203, Sakurai teaches to perform an ion implantation using an implantation energy of 400 KeV (1×10^{15} atoms/cm^2) (page 11, lines 32 to 35). As discussed above, Sakurai produces a trough using an energy that would allow the upper inner area to change the doping, i.e. the inner surface area of a p-doped substrate will become an n-doped inner surface area or vice versa.

I^2L elements (gates) with multiple connector outputs are inverse operating npn transistors. The trough is grounded and serves as an emitter. The doping concentration of this emitter has to be very high to guarantee sufficient amplification in the inverse mode. Sakurai uses a comparatively low n-type implantation energy of 400 KeV and a dose of $1 \times 10^{15}/cm^2$ for the implantation of a p-substrate with a doping concentration of $1 \times 10^{15}/cm^3$. Therefore, the trough will be completely filled up to the surface with the implanted species. That means a p-doped base has to be implanted in an additional process step to overcompensate the doping of the n-trough in the base region. Sakurai teaches to use an ion implantation for obtaining the p-type regions 204, 205 (page 11, line 35 to page 12, line 1). In order to get a sufficiently high implantation, the overcompensation has to be done very carefully. Such a process is not easy to

control and suffers from yield problems. In such a configuration, only lateral injection pnp-transistors with low amplification are possible.

In contrast to Sakurai, the trough in the substrate according to the invention is produced by means of an ion implantation using an energy that will assure that there is no turnover of conductivity type, e.g. 6 MeV ($2 \times 10^{13}/cm^2$). It should be noted that the trough produced by means of such an ion implantation is characterized by a comparatively low doping. An I^2L element could never work with such a low doped n-trough as an emitter and a traditional implanted base as taught by Sakurai. In this case, the inversely working npn-transistor needs super-beta amplification. It is well known that these transistors have low yield in production. In case n-trough implantation energy dose and substrate doping are carefully matched, the remaining p-region of the n-trough may be used as the base of the inverse working npn transistor with super-beta characteristics. But this is not the principle of the invention.

According to the invention, the p-doped inner area forms the base of the multi-collector transistor rather than an additional implantation as taught by Sakurai. The base of the I^2L element according to the invention has the lowest possible doping concentration, namely substrate concentration, e.g. $2 \times 10^{15}/cm^3$. Only in connection with this base, the low n-trough doping is acceptable. From the production point of view, a low implantation dose of the n-trough has further advantages. High energy implantation is costly. Generating the base in the proposed manner guarantees high yield and is very reproducible. There is no need for an additional base implantation step and the base silicon of the npn transistor is nearly undisturbed because the high energy ions pass through without leaving traces. In addition, this base zone can also be used as a collector of a pnp injector. This pnp transistor has a vertical structure with high amplification rather than the lateral structure as taught by Sakurai.

In contrast to the prior art, also the pnp transistor and the field effect transistor according to the invention have further advantages.

Concerning the field effect transistor (JFET), it is absolutely unexpected that this device has a threshold voltage of less than 1 V, a breakdown voltage of up to 70 V, and a remarkably low temperature drift of only a few 100 ppm/K. The reason for the low threshold voltage is the low doping concentration of the channel of this device, which is defined by the concentration of the substrate, which means a low concentration, and not -- like in conventional devices -- by additional implantations. This allows simple, nearly perfect current sources in the bipolar

technology, better than in CMOS technologies as well, with a very high yield. Until now bipolar analog designs suffer from the lack of such an element. Now the designs could be smaller and easier to be developed with the help of this JFET element.

The pnp transistor fabricated with the method according to the invention has a breakdown voltage of up to 70 V with open base and base-shorted to emitter, at an amplification of 130 and a transit frequency of 160 MHz.

All elements described in the patent application can be produced with the same parameter set of high energy implantations, dose and substrate concentrations; that means in the same production cycle.

For all of the above reasons, the claims pending in this application are believed to be in condition for allowance, and such action is respectfully requested.

If it would advance the prosecution of this application, the Examiner is invited to contact Applicant's attorney at the below indicated telephone number.

Respectfully submitted,

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Dated: August 5, 2003

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